WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell array including a plurality of blocks, each of the blocks including memory cells arranged in rows and columns;

a block select circuit configured to select one of the blocks of the memory cell array;

a plurality of word-line-driving-signal lines to receive voltages to be applied to a plurality of word lines in each block; and

a plurality of transfer transistors having current paths thereof connected between the word-line-driving-signal lines and the word lines of the each block, the transfer transistors being controlled by outputs from the block select circuit, any two of the transfer transistors, which correspond to each pair of adjacent ones of the word lines, being separate from each other lengthwise and widthwise, one or more transfer transistors corresponding to another word line or other word lines being interposed between the any two transfer transistors.

2. The semiconductor memory device according to claim 1, wherein address numbers assigned to word lines connected to adjacent ones of the transfer transistors are separate from each other by 2 or more.

3. The semiconductor memory device according to claim 1, wherein a first element-isolation region,

which is interposed between word-line-side terminals of some of the transfer transistors in the each block, has a narrower width than a second element-isolation region, which is interposed between word-line-side terminals and word-line-driving-signal line-side terminals of other transfer transistors in the each block.

4. The semiconductor memory device according to claim 1, wherein wires are led from word-line-side terminals of the transfer transistors in the each block to the respective word lines of the memory cell array such that the wires are ordered with respect to the word lines.

5. The semiconductor memory device according to claim 1, wherein wires led from word-line-side terminals of the transfer transistors in the each block to the respective word lines of the memory cell array is formed of a metal wiring layer provided above and closest to a wiring layer that is formed into the word lines.

6. The semiconductor memory device according to claim 1, wherein the block select circuit includes a decoder section configured to decode row addresses assigned to the memory cell array, or pre-decode signals related to the row addresses, and a booster section configured to receive decode signals output from the decoder section.

7. The semiconductor memory device according to

claim 1, wherein the each block further includes first and second select transistors having gates thereof connected to respective ends of current paths of corresponding ones of the transfer transistors, and memory cells having current paths thereof connected in series between the first and second select transistors, and the memory cells also having gates thereof connected to respective ends of current paths of corresponding ones of the transfer transistors.

8. A semiconductor memory device comprising:

a memory cell array including a plurality of blocks, each of the blocks including memory cells arranged in rows and columns;

a block select circuit configured to select one of the blocks of the memory cell array;

a plurality of word-line-driving-signal lines to receive voltages to be applied to a plurality of word lines in each block; and

a plurality of transfer transistors connected between the word-line-driving-signal lines and the word lines of the memory cell array, the transfer transistors being controlled by outputs from the block select circuit, a first element-isolation region, interposed between word-line-side terminals of some of the transfer transistors in the each block, having a narrower width than a second element-isolation region, interposed between word-line-side terminals and

word-line-driving-signal line-side terminals of other transfer transistors in the each block.

9. The semiconductor memory device according to claim 8, wherein wires are led from word-line-side terminals of the transfer transistors in the each block to the respective word lines of the memory cell array such that the wires are ordered with respect to the word lines.

10. The semiconductor memory device according to claim 8, wherein wires led from word-line-side terminals of the transfer transistors in the each block to the respective word lines of the memory cell array is formed of a metal wiring layer provided above and closest to a wiring layer that is formed into the word lines.

11. The semiconductor memory device according to claim 8, wherein the block select circuit includes a decoder section configured to decode row addresses assigned to the memory cell array, or pre-decode signals related to the row addresses, and a booster section configured to receive decode signals output from the decoder section.

12. The semiconductor memory device according to claim 8, wherein the each block further includes first and second select transistors having gates thereof connected to respective ends of current paths of corresponding ones of the transfer transistors, and

memory cells having current paths thereof connected in series between the first and second select transistors, and the memory cells also having gates thereof connected to respective ends of current paths of corresponding ones of the transfer transistors.

13. A semiconductor memory device comprising:

a memory cell array including electrically programmable nonvolatile memory cells arranged in rows and columns;

block select means for selecting one of blocks that are included in the memory cell array and each have a plurality of word lines;

a plurality of word-line-driving-signal lines to receive voltages to be applied to a plurality of word lines in each block; and

a plurality of transfer transistors having current paths thereof connected between the word-line-driving-signal lines and the word lines of the each block, the transfer transistors being controlled by outputs from the block select means,

wherein any two of the transfer transistors, which correspond to each pair of adjacent ones of the word lines, are separate from each other lengthwise and widthwise, and one or more transfer transistors corresponding to another word line or other word lines are interposed between the any two transfer transistors.

14. The semiconductor memory device according to

claim 13, wherein address numbers assigned to word lines connected to adjacent ones of the transfer transistors are separate from each other by 2 or more.

15. The semiconductor memory device according to claim 13, wherein a first element-isolation region, which is interposed between word-line-side terminals of some of the transfer transistors in the each block, has a narrower width than a second element-isolation region, which is interposed between word-line-side terminals and word-line-driving-signal line-side terminals of other transfer transistors in the each block.

16. The semiconductor memory device according to claim 13, wherein wires are led from word-line-side terminals of the transfer transistors in the each block to the respective word lines of the memory cell array such that the wires are ordered with respect to the word lines.

17. The semiconductor memory device according to claim 13, wherein wires led from word-line-side terminals of the transfer transistors in the each block to the respective word lines of the memory cell array is formed of a metal wiring layer provided above and closest to a wiring layer that is formed into the word lines.

18. The semiconductor memory device according to claim 13, wherein the block select means includes a decoder section configured to decode row addresses

assigned to the memory cell array, or pre-decode signals related to the row addresses, and a booster section configured to receive decode signals output from the decoder section.

19. The semiconductor memory device according to claim 13, wherein the each block further includes first and second select transistors having gates thereof connected to respective ends of current paths of corresponding ones of the transfer transistors, and memory cells having current paths thereof connected in series between the first and second select transistors, and the memory cells also having gates thereof connected to respective ends of current paths of corresponding ones of the transfer transistors.

20. A semiconductor memory device comprising:

a memory cell array including electrically programmable nonvolatile memory cells arranged in rows and columns;

block select means for selecting one of blocks that are included in the memory cell array and each have a plurality of word lines;

a plurality of word-line-driving-signal lines to receive voltages to be applied to a plurality of word lines in each block; and

a plurality of transfer transistors connected between the word-line-driving-signal lines and the word lines of the memory cell array, the transfer

transistors being controlled by outputs from the block select means,

wherein a first element-isolation region, which is interposed between word-line-side terminals of some of the transfer transistors in the each block, has a narrower width than a second element-isolation region, which is interposed between word-line-side terminals and word-line-driving-signal line-side terminals of other transfer transistors in the each block.

21. The semiconductor memory device according to claim 20, wherein wires are led from word-line-side terminals of the transfer transistors in the each block to the respective word lines of the memory cell array such that the wires are ordered with respect to the word lines.

22. The semiconductor memory device according to claim 20, wherein wires led from word-line-side terminals of the transfer transistors in the each block to the respective word lines of the memory cell array is formed of a metal wiring layer provided above and closest to a wiring layer that is formed into the word lines.

23. The semiconductor memory device according to claim 20, wherein the block select means includes a decoder section configured to decode row addresses assigned to the memory cell array, or pre-decode signals related to the row addresses, and a booster

section configured to receive decode signals output from the decoder section.

24. The semiconductor memory device according to claim 20, wherein the each block further includes first and second select transistors having gates thereof connected to respective ends of current paths of corresponding ones of the transfer transistors, and memory cells having current paths thereof connected in series between the first and second select transistors, and the memory cells also having gates thereof connected to respective ends of current paths of corresponding ones of the transfer transistors.

25. A semiconductor memory device comprising:

a memory cell array including a plurality of blocks, each of the blocks including electrically programmable nonvolatile memory cells arranged in rows and columns;

a plurality of word-line-driving-signal lines to receive voltages to be applied to a plurality of word lines in each block; and

block select circuit configured to select one of blocks that are included in the memory cell array and each have a plurality of word lines, the block select circuit includes a decoder section configured to decode row addresses assigned to the memory cell array, or pre-decode signals related to the row addresses, and a booster section configured to receive decode signals

output from the decoder section,

wherein any two of the transfer transistors, which correspond to each pair of adjacent ones of the word lines, are separate from each other lengthwise and widthwise, and one or more transfer transistors corresponding to another word line or other word lines are interposed between the any two transfer transistors.

26. The semiconductor memory device according to claim 25, wherein address numbers assigned to word lines connected to adjacent ones of the transfer transistors are separate from each other by 2 or more.

27. The semiconductor memory device according to claim 25, wherein a first element-isolation region, which is interposed between word-line-side terminals of some of the transfer transistors in the each block, has a narrower width than a second element-isolation region, which is interposed between word-line-side terminals and word-line-driving-signal line-side terminals of other transfer transistors in the each block.

28. The semiconductor memory device according to claim 25, wherein wires are led from word-line-side terminals of the transfer transistors in the each block to the respective word lines of the memory cell array such that the wires are ordered with respect to the word lines.

29. The semiconductor memory device according to claim 25, wherein wires led from word-line-side

terminals of the transfer transistors in the each block to the respective word lines of the memory cell array is formed of a metal wiring layer provided above and closest to a wiring layer that is formed into the word lines.

30. The semiconductor memory device according to claim 25, wherein the each block further includes first and second select transistors having gates thereof connected to respective ends of current paths of corresponding ones of the transfer transistors, and memory cells having current paths thereof connected in series between the first and second select transistors, and the memory cells also having gates thereof connected to respective ends of current paths of corresponding ones of the transfer transistors.